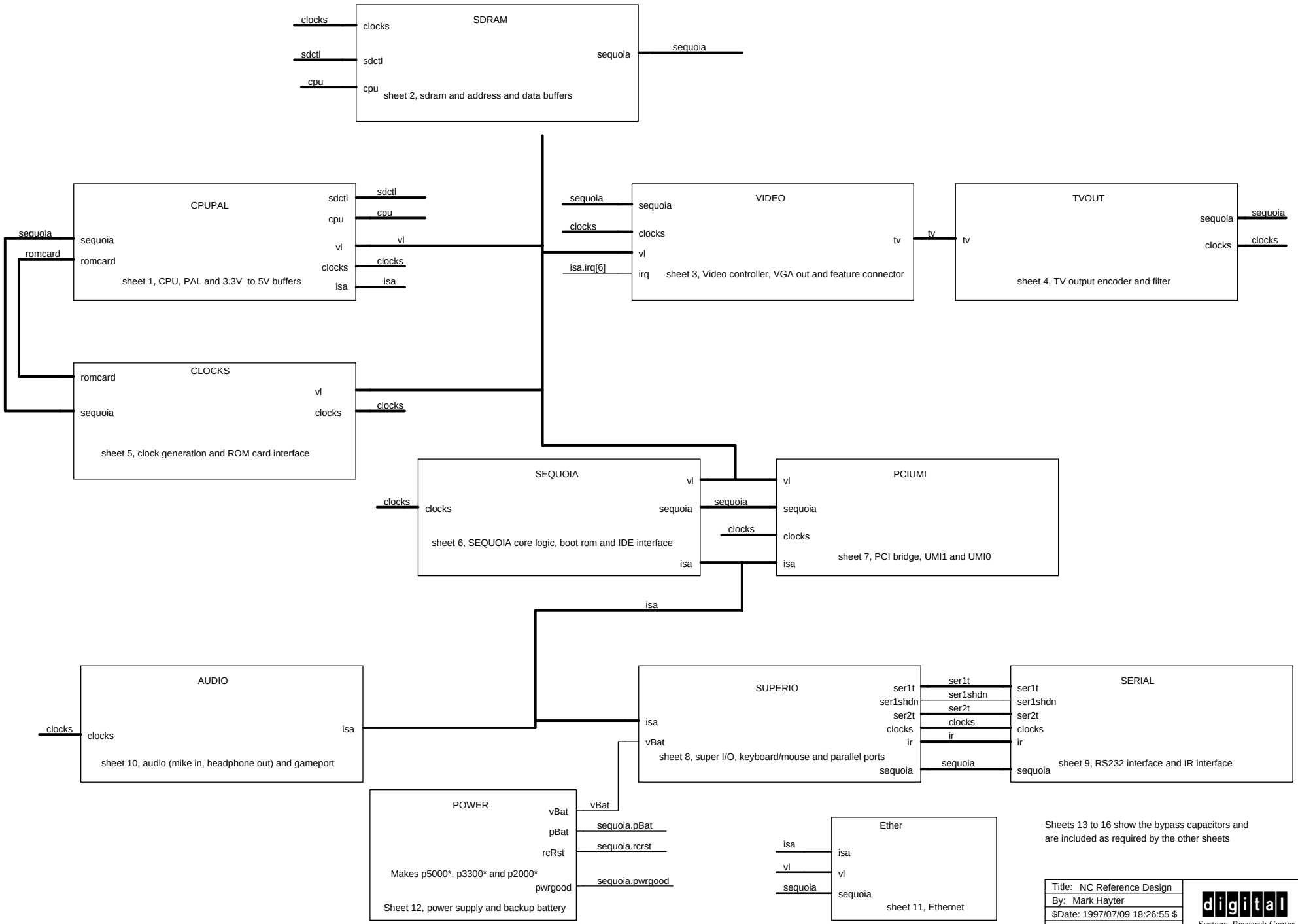
SDRAM
clocks
sdctl
cpu
sequoia
sheet 2, sdram and address and data buffers
CPUPAL
sequoia
romcard
vl
clocks
isa
sheet 1, CPU, PAL and 3.3V to 5V buffers
VIDEO
irq
tv
sheet 3, Video controller, VGA out and feature connector
TVOUT
sheet 4, TV output encoder and filter
CLOCKS
sheet 5, clock generation and ROM card interface
SEQUOIA
sheet 6, SEQUOIA core logic, boot rom and IDE interface
PCIUMI
sheet 7, PCI bridge, UMI1 and UMI0
AUDIO
sheet 10, audio (mike in, headphone out) and gameport
SUPERIO
vBat
sheet 8, super I/O, keyboard/mouse and parallel ports
SERIAL
ser1t
ser1shdn
ser2t
ir
sheet 9, RS232 interface and IR interface
POWER
pBat
rcRst
pwrgood
Makes p5000*, p3300* and p2000*
Sheet 12, power supply and backup battery
sequoia.pBat
sequoia.rcrst
sequoia.pwrgood
Ether
sheet 11, Ethernet
isa.irq[6]
Sheets 13 to 16 show the bypass capacitors and
are included as required by the other sheets
Title: NC Reference Design
By: Mark Hayter
$Date: 1997/07/09 18:26:55 $
RCS $Revision: 1.21 $
Version: Rev 5
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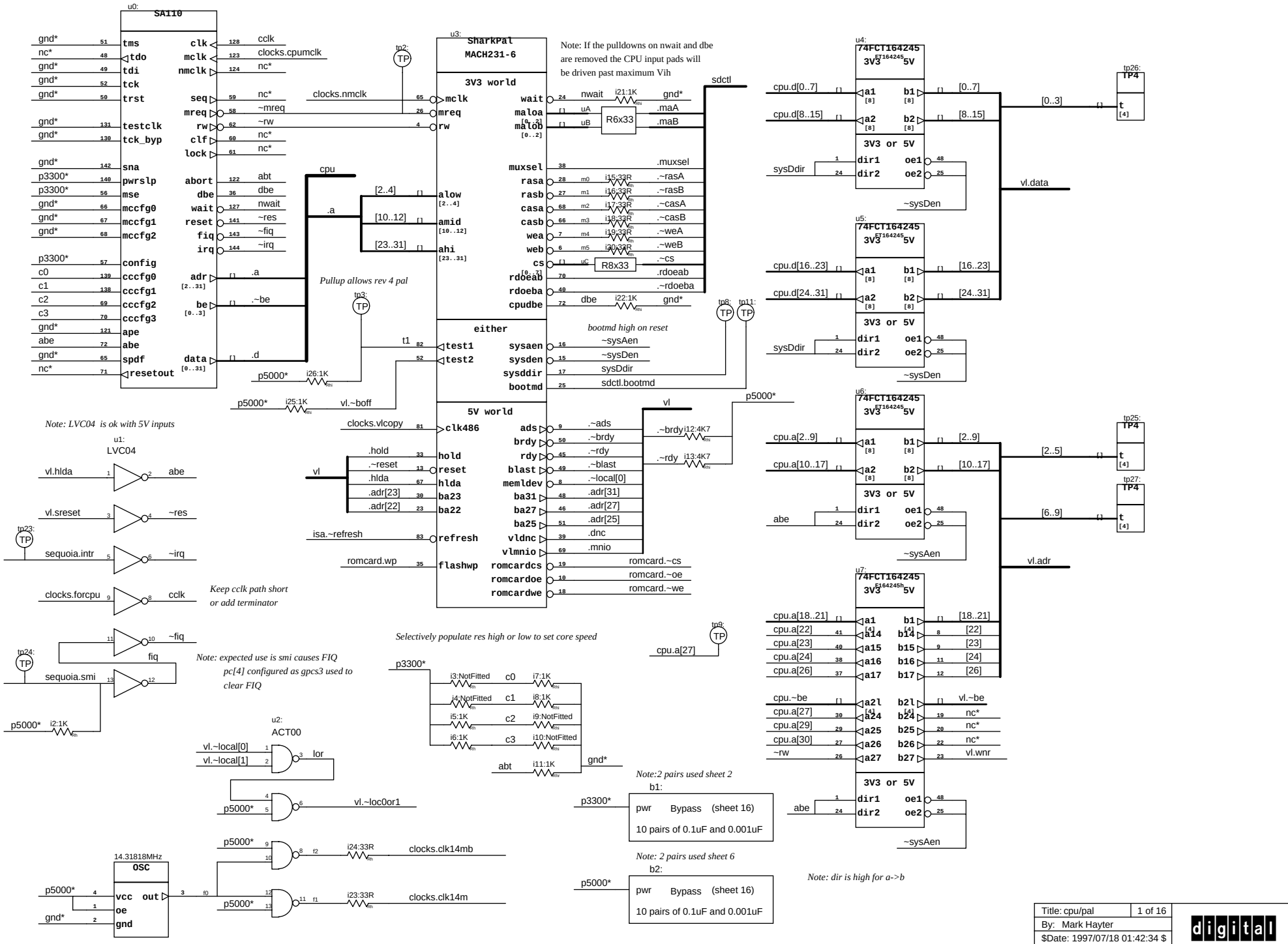
Palo Alto, CA



Title: cpu/pal	1 of 16
By: Mark Hayter	
$Date: 1997/07/18 01:42:34 $	
RCS $Revision: 1.39 $	
Version: Rev 5	

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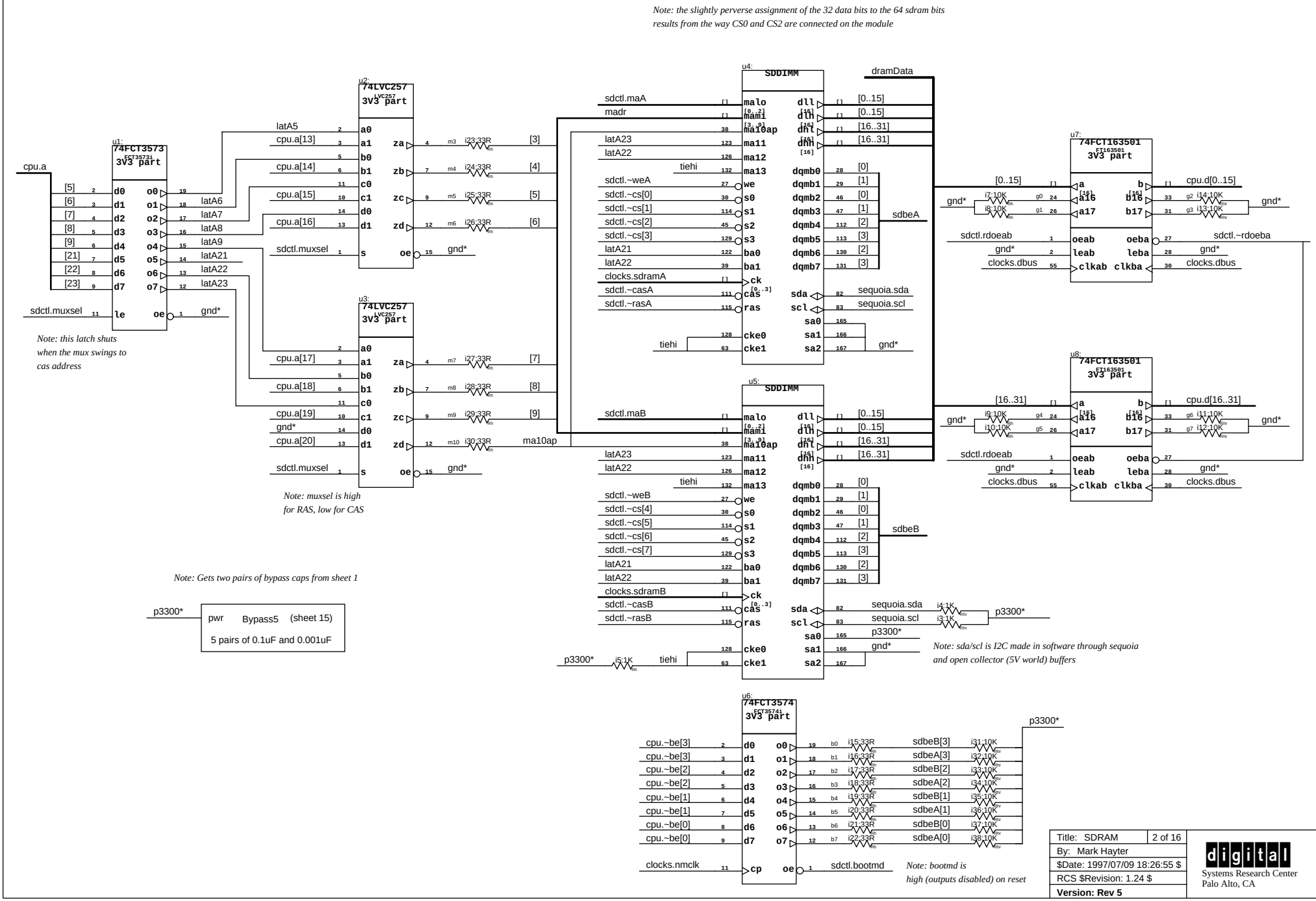
Palo Alto, CA


Note: the slightly perverse assignment of the 32 data bits to the 64 sdram bits results from the way CS0 and CS2 are connected on the module
u1: 74FCT3573 3V3 part
u2: 74LVC257 3V3 part
u3: 74LVC257 3V3 part
u4: SDDIMM
u5: SDDIMM
u6: 74FCT3574 3V3 part
u7: 74FCT163501 3V3 part
u8: 74FCT163501 3V3 part
dramData
cpu.a
latA5
latA6
latA7
latA8
latA9
latA21
latA22
latA23
sdctl.muxsel
gnd*
Note: this latch shuts when the mux swings to cas address
Note: muxsel is high for RAS, low for CAS
ma10ap
sdctl.maA
sdctl.maB
madr
sdctl.~weA
sdctl.~weB
sdctl.~cs[0]
sdctl.~cs[1]
sdctl.~cs[2]
sdctl.~cs[3]
sdctl.~cs[4]
sdctl.~cs[5]
sdctl.~cs[6]
sdctl.~cs[7]
sdctl.~casA
sdctl.~casB
sdctl.~rasA
sdctl.~rasB
clocks.sdramA
clocks.sdramB
tiehi
sdbeA
sdbeB
sequoia.sda
sequoia.scl
p3300*
Note: sda/scl is I2C made in software through sequoia and open collector (5V world) buffers
Note: Gets two pairs of bypass caps from sheet 1
pwr Bypass5 (sheet 15)
5 pairs of 0.1uF and 0.001uF
cpu.~be[3]
cpu.~be[2]
cpu.~be[1]
cpu.~be[0]
clocks.nmclk
sdctl.bootmd
sdbeA[3]
sdbeA[2]
sdbeA[1]
sdbeA[0]
sdbeB[3]
sdbeB[2]
sdbeB[1]
sdbeB[0]
Note: bootmd is high (outputs disabled) on reset
cpu.d[0..15]
cpu.d[16..31]
sdctl.rdoeab
sdctl.~rdoeba
clocks.dbus
Title: SDRAM
2 of 16
By: Mark Hayter
$Date: 1997/07/09 18:26:55 $
RCS $Revision: 1.24 $
Version: Rev 5
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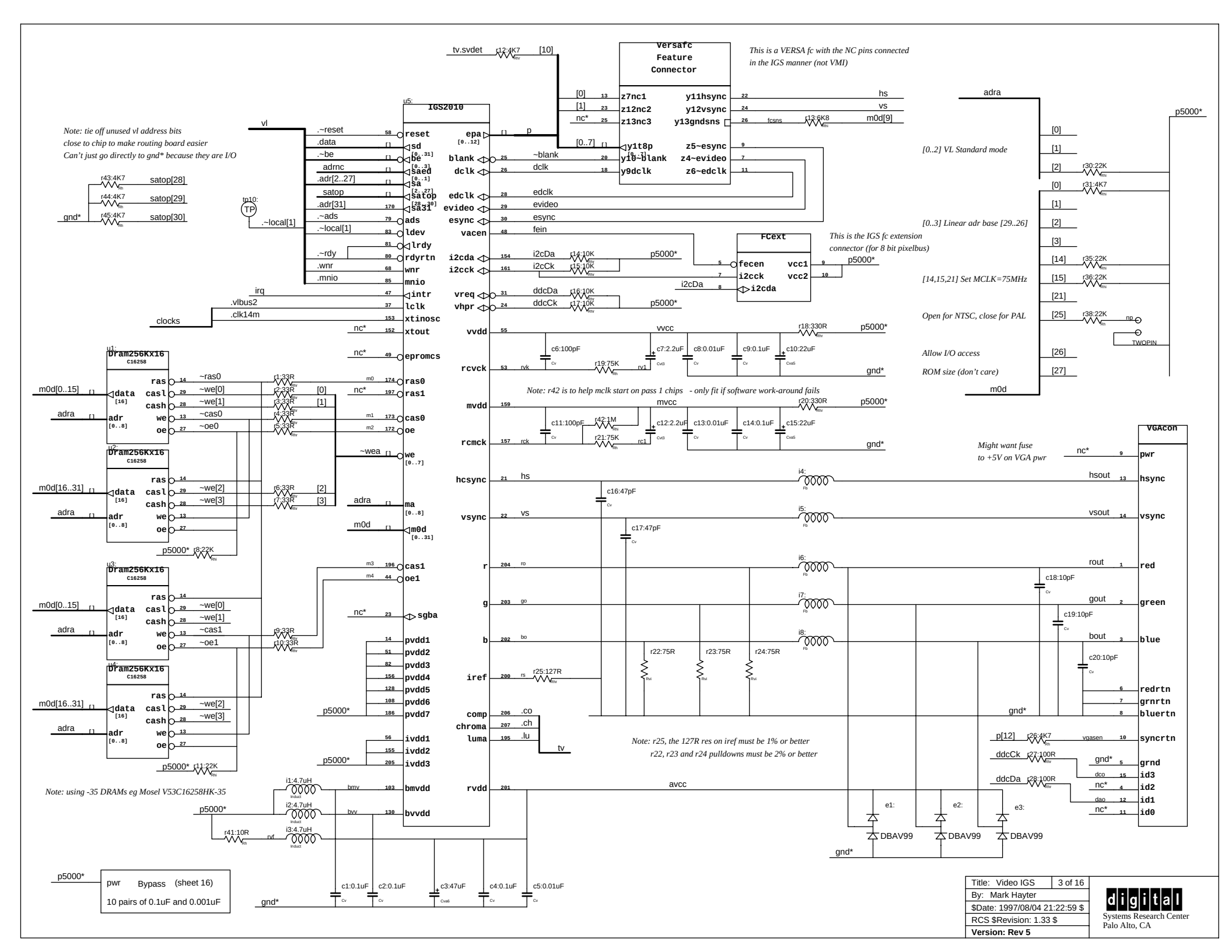
Versafc Feature Connector
This is a VERSA fc with the NC pins connected in the IGS manner (not VMI)
IGS2010
u5:
Note: tie off unused vl address bits close to chip to make routing board easier
Can't just go directly to gnd* because they are I/O
[0..2] VL Standard mode
[0..3] Linear adr base [29..26]
[14,15,21] Set MCLK=75MHz
Open for NTSC, close for PAL
Allow I/O access
ROM size (don't care)
This is the IGS fc extension connector (for 8 bit pixelbus)
FCext
Note: r42 is to help mclk start on pass 1 chips - only fit if software work-around fails
Might want fuse to +5V on VGA pwr
VGAcon
Note: r25, the 127R res on iref must be 1% or better
r22, r23 and r24 pulldowns must be 2% or better
Note: using -35 DRAMs eg Mosel V53C16258HK-35
DBAV99
pwr Bypass (sheet 16)
10 pairs of 0.1uF and 0.001uF
Title: Video IGS
3 of 16
By: Mark Hayter
$Date: 1997/08/04 21:22:59 $
RCS $Revision: 1.33 $
Version: Rev 5
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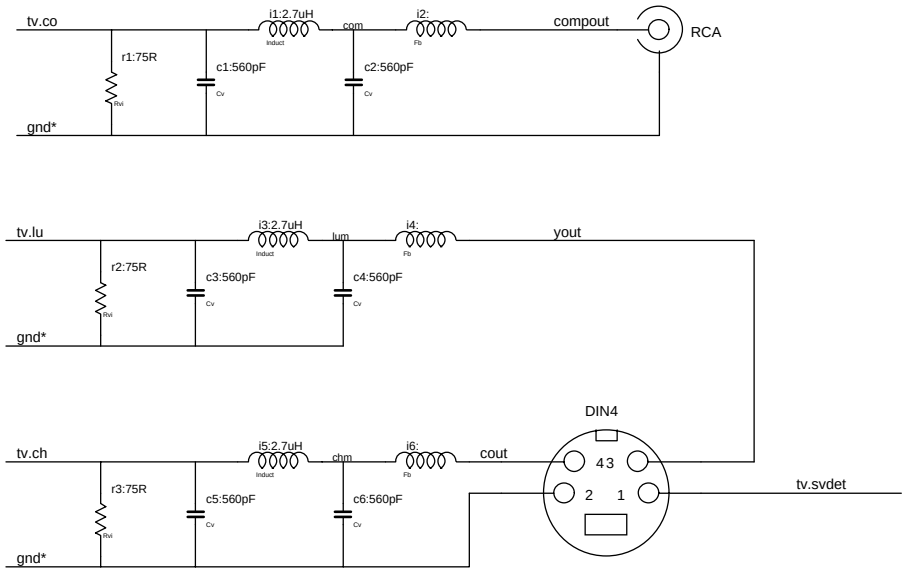

Title: TV out IGS	4 of 16
By: Mark Hayter	
$Date: 1997/07/09 18:26:55 $	
RCS $Revision: 1.13 $	
Version: Rev 5	

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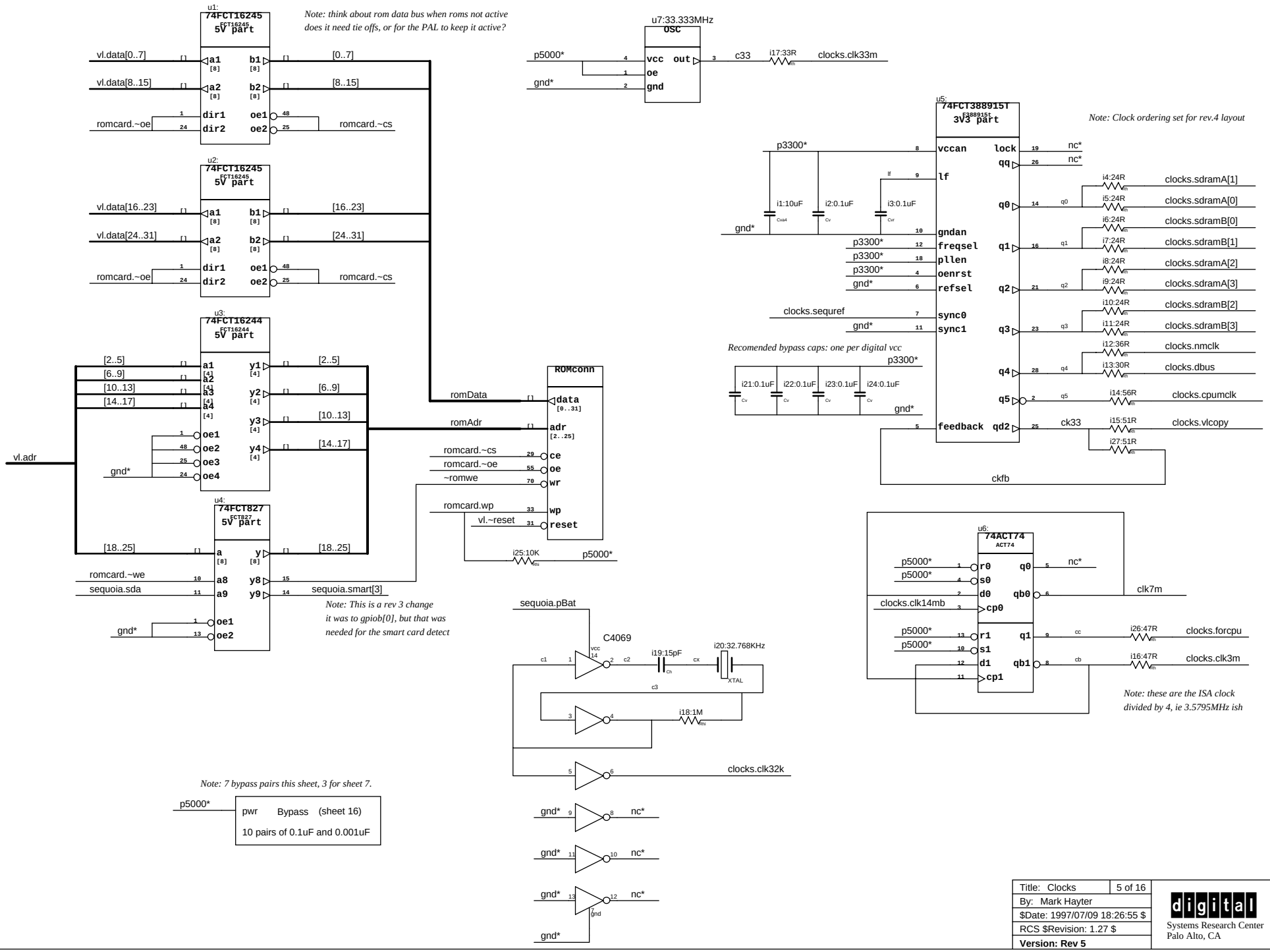

Title: Clocks	5 of 16
By: Mark Hayter	
$Date: 1997/07/09 18:26:55 $	
RCS $Revision: 1.27 $	
Version: Rev 5	

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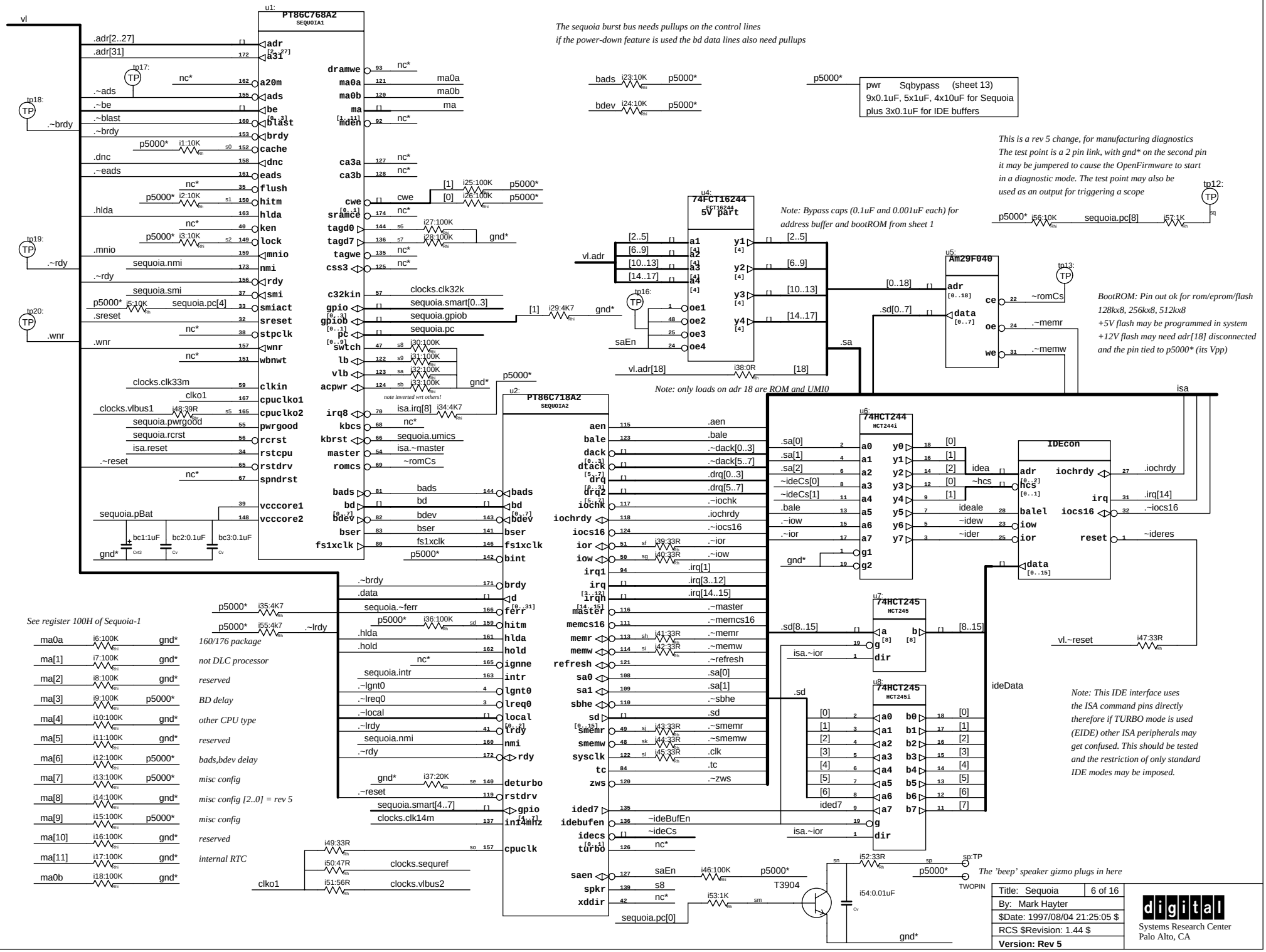
Systems Research Center
Palo Alto, CA


The sequoia burst bus needs pullups on the control lines
if the power-down feature is used the bd data lines also need pullups
pwr Sqbypass (sheet 13)
9x0.1uF, 5x1uF, 4x10uF for Sequoia
plus 3x0.1uF for IDE buffers
This is a rev 5 change, for manufacturing diagnostics
The test point is a 2 pin link, with gnd* on the second pin
it may be jumpered to cause the OpenFirmware to start
in a diagnostic mode. The test point may also be
used as an output for triggering a scope
Note: Bypass caps (0.1uF and 0.001uF each) for
address buffer and bootROM from sheet 1
BootROM: Pin out ok for rom/eprom/flash
128kx8, 256kx8, 512kx8
+5V flash may be programmed in system
+12V flash may need adr[18] disconnected
and the pin tied to p5000* (its Vpp)
Note: only loads on adr 18 are ROM and UMI0
Note: This IDE interface uses
the ISA command pins directly
therefore if TURBO mode is used
(EIDE) other ISA peripherals may
get confused. This should be tested
and the restriction of only standard
IDE modes may be imposed.
The 'beep' speaker gizmo plugs in here
See register 100H of Sequoia-1
160/176 package
not DLC processor
reserved
BD delay
other CPU type
reserved
bads,bdev delay
misc config
misc config [2..0] = rev 5
misc config
reserved
internal RTC
u1: PT86C768A2 SEQUOIA1
u2: PT86C718A2 SEQUOIA2
u4: 74FCT16244 5V part
u5: Am29F040
u6: 74HCT244
u7: 74HCT245
u8: 74HCT245
IDEcon
T3904
Title: Sequoia 6 of 16
By: Mark Hayter
$Date: 1997/08/04 21:25:05 $
RCS $Revision: 1.44 $
Version: Rev 5
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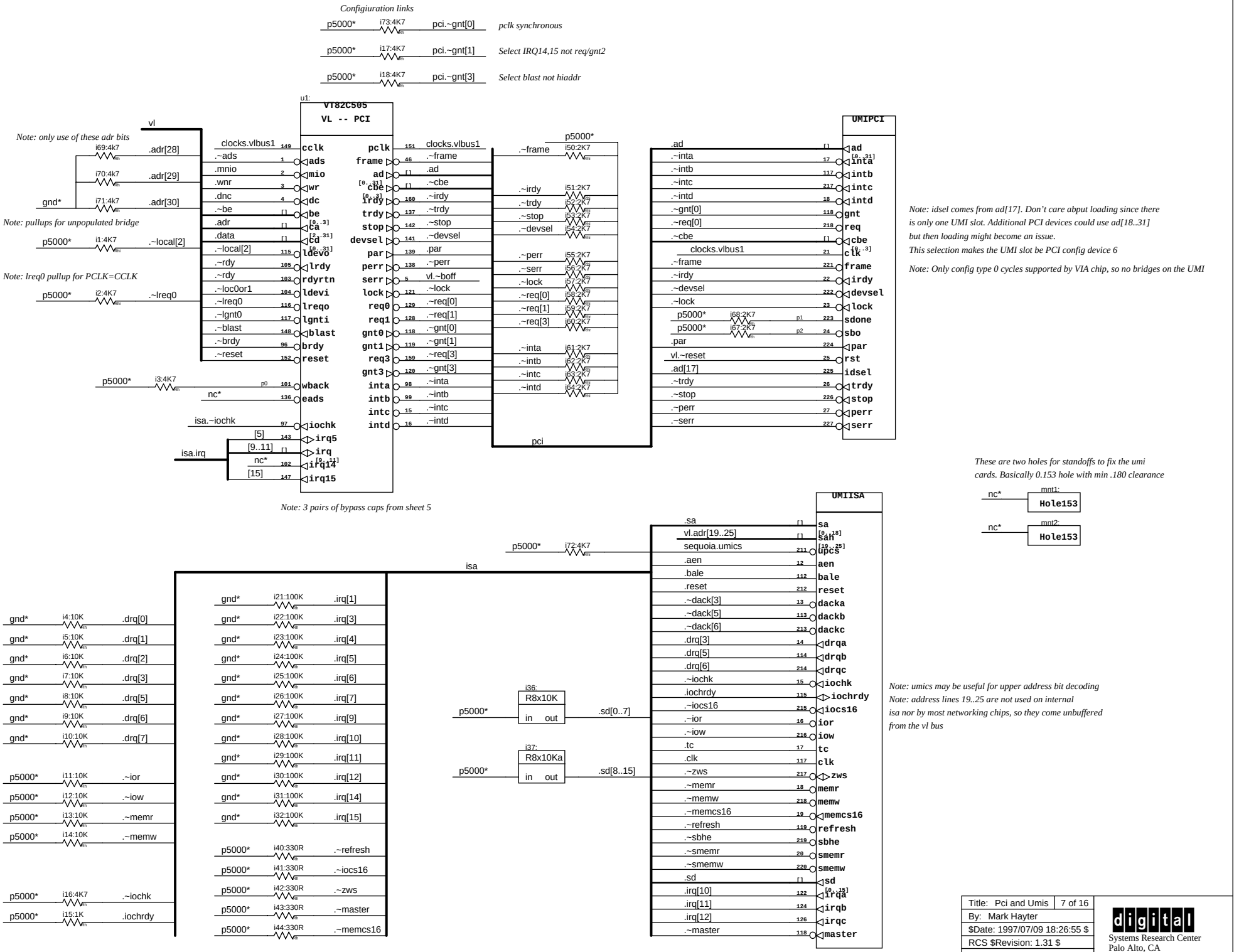
Configiuration links
p5000* i73:4K7 pci.~gnt[0] pclk synchronous
p5000* i17:4K7 pci.~gnt[1] Select IRQ14,15 not req/gnt2
p5000* i18:4K7 pci.~gnt[3] Select blast not hiaddr
u1:
VT82C505
VL -- PCI
vl
Note: only use of these adr bits
i69:4K7 .adr[28]
i70:4K7 .adr[29]
gnd* i71:4K7 .adr[30]
Note: pullups for unpopulated bridge
p5000* i1:4K7 .~local[2]
Note: lreq0 pullup for PCLK=CCLK
p5000* i2:4K7 .~lreq0
clocks.vlbus1 149 cclk
.~ads 1 ads
.mnio 2 mio
.wnr 3 wr
.dnc 4 dc
.~be [] be
.adr [0..3] ca
.data [2..31] cd
.~local[2] 115 ldevo
.~rdy 105 lrdy
.~rdy 103 rdyrtn
.~loc0or1 104 ldevi
.~lreq0 116 lreqo
.~lgnt0 117 lgnti
.~blast 148 blast
.~brdy 96 brdy
.~reset 152 reset
p5000* i3:4K7 p0 101 wback
nc* 136 eads
isa.~iochk 97 iochk
[5] 143 irq5
[9..11] [] irq [9..12]
isa.irq nc* 102 irq14
[15] 147 irq15
pclk 151 clocks.vlbus1
frame 46 .~frame
ad [] .ad
cbe [0..31] [] .~cbe
irdy [0..3] 160 .~irdy
trdy 137 .~trdy
stop 142 .~stop
devsel 141 .~devsel
par 139 .par
perr 138 .~perr
serr 5 vl.~boff
lock 121 .~lock
req0 129 .~req[0]
req1 128 .~req[1]
gnt0 118 .~gnt[0]
gnt1 119 .~gnt[1]
req3 159 .~req[3]
gnt3 120 .~gnt[3]
inta 98 .~inta
intb 99 .~intb
intc 15 .~intc
intd 16 .~intd
p5000*
.~frame i50:2K7
.~irdy i51:2K7
.~trdy i52:2K7
.~stop i53:2K7
.~devsel i54:2K7
.~perr i55:2K7
.~serr i56:2K7
.~lock i57:2K7
.~req[0] i58:2K7
.~req[1] i59:2K7
.~req[3] i60:2K7
.~inta i61:2K7
.~intb i62:2K7
.~intc i63:2K7
.~intd i64:2K7
pci
UMIPCI
.ad [] ad
.~inta 17 inta [0..31]
.~intb 117 intb
.~intc 217 intc
.~intd 18 intd
.~gnt[0] 118 gnt
.~req[0] 218 req
.~cbe [] cbe
clocks.vlbus1 21 clk [0..3]
.~frame 221 frame
.~irdy 22 irdy
.~devsel 222 devsel
.~lock 23 lock
p5000* i68:2K7 p1 223 sdone
p5000* i67:2K7 p2 24 sbo
.par 224 par
vl.~reset 25 rst
.ad[17] 225 idsel
.~trdy 26 trdy
.~stop 226 stop
.~perr 27 perr
.~serr 227 serr
Note: 3 pairs of bypass caps from sheet 5
Note: idsel comes from ad[17]. Don't care abput loading since there is only one UMI slot. Additional PCI devices could use ad[18..31] but then loading might become an issue. This selection makes the UMI slot be PCI config device 6
Note: Only config type 0 cycles supported by VIA chip, so no bridges on the UMI
These are two holes for standoffs to fix the umi cards. Basically 0.153 hole with min .180 clearance
nc* mnt1: Hole153
nc* mnt2: Hole153
UMIISA
isa
p5000* i72:4K7 sequoia.umics 211 upcs
.aen 12 aen
.bale 112 bale
.reset 212 reset
.~dack[3] 13 dacka
.~dack[5] 113 dackb
.~dack[6] 213 dackc
.drq[3] 14 drqa
.drq[5] 114 drqb
.drq[6] 214 drqc
.~iochk 15 iochk
.iochrdy 115 iochrdy
.~iocs16 215 iocs16
.~ior 16 ior
.~iow 216 iow
.tc 17 tc
.clk 117 clk
.~zws 217 zws
.~memr 18 memr
.~memw 218 memw
.~memcs16 19 memcs16
.~refresh 119 refresh
.~sbhe 219 sbhe
.~smemr 20 smemr
.~smemw 220 smemw
.sa [] sa [0..8]
vl.adr[19..25] [] san [19..25]
.sd [] sd [0..15]
.irq[10] 122 irqa
.irq[11] 124 irqb
.irq[12] 126 irqc
.~master 118 master
i36: R8x10K in out p5000* .sd[0..7]
i37: R8x10Ka in out p5000* .sd[8..15]
gnd* i4:10K .drq[0]
gnd* i5:10K .drq[1]
gnd* i6:10K .drq[2]
gnd* i7:10K .drq[3]
gnd* i8:10K .drq[5]
gnd* i9:10K .drq[6]
gnd* i10:10K .drq[7]
p5000* i11:10K .~ior
p5000* i12:10K .~iow
p5000* i13:10K .~memr
p5000* i14:10K .~memw
p5000* i16:4K7 .~iochk
p5000* i15:1K .iochrdy
gnd* i21:100K .irq[1]
gnd* i22:100K .irq[3]
gnd* i23:100K .irq[4]
gnd* i24:100K .irq[5]
gnd* i25:100K .irq[6]
gnd* i26:100K .irq[7]
gnd* i27:100K .irq[9]
gnd* i28:100K .irq[10]
gnd* i29:100K .irq[11]
gnd* i30:100K .irq[12]
gnd* i31:100K .irq[14]
gnd* i32:100K .irq[15]
p5000* i40:330R .~refresh
p5000* i41:330R .~iocs16
p5000* i42:330R .~zws
p5000* i43:330R .~master
p5000* i44:330R .~memcs16
Note: umics may be useful for upper address bit decoding
Note: address lines 19..25 are not used on internal isa nor by most networking chips, so they come unbuffered from the vl bus
Title: Pci and Umis
7 of 16
By: Mark Hayter
$Date: 1997/07/09 18:26:55 $
RCS $Revision: 1.31 $
Version: Rev 5
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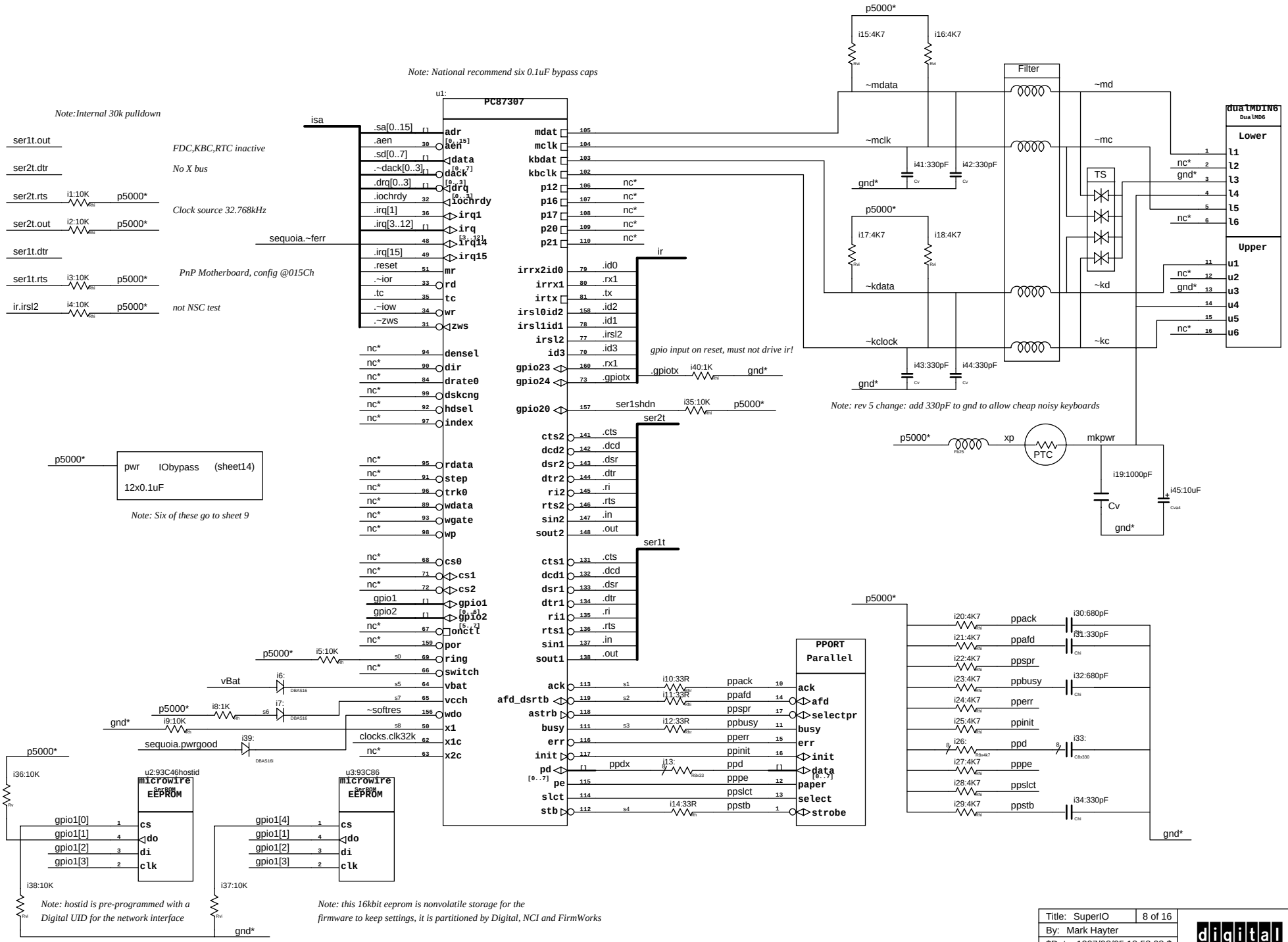

Title: SuperIO	8 of 16
By: Mark Hayter	
$Date: 1997/08/05 18:58:08 $	
RCS $Revision: 1.34 $	
Version: Rev 5	

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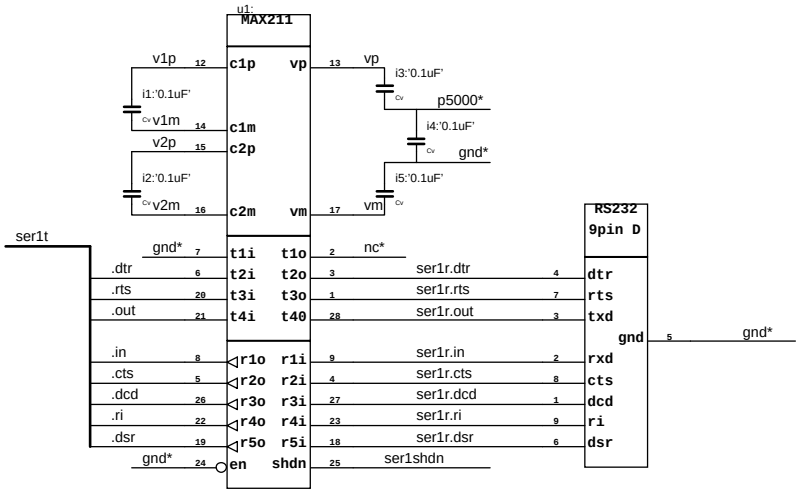
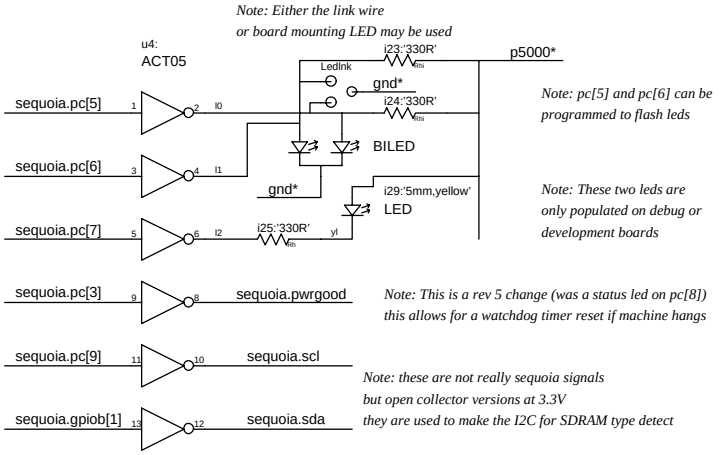


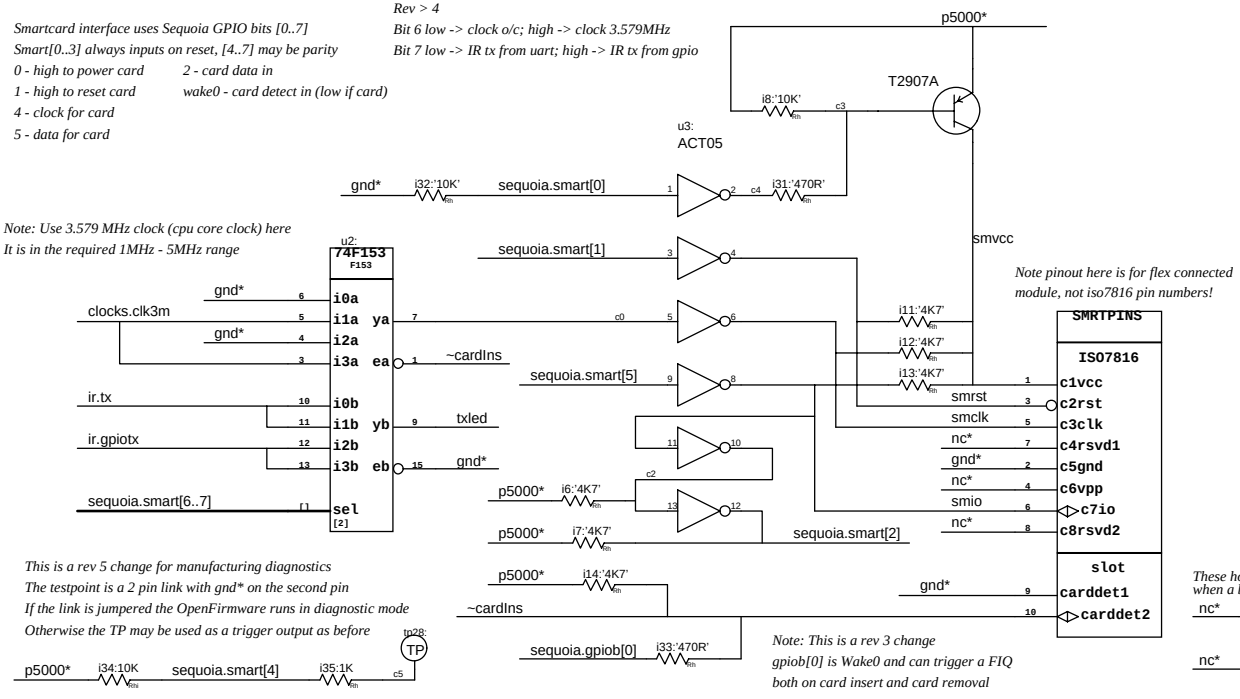


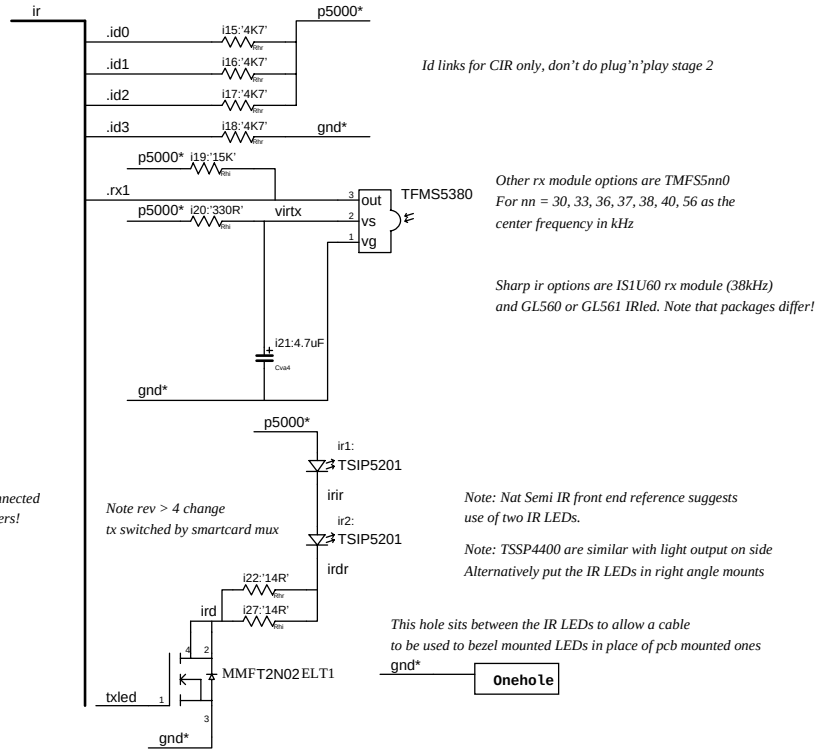
The IR from the SuperIO supports IRDA and Consumer IR
Only 38kHz consumer IR is provided here
TX frequency is set by software, but receiver module is tuned

Rev <=4
7 6
0 0 data, clock o/c
0 1 3.579MHz clock, gpio data
1 0 gpio clock, gpio data
1 1 3.579MHz clock, uart

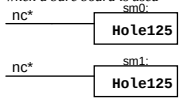
Rev > 4
Bit 6 low -> clock o/c; high -> clock 3.579MHz
Bit 7 low -> IR tx from uart; high -> IR tx from gpio

Smartcard interface uses Sequoia GPIO bits [0..7]
Smart[0..3] always inputs on reset, [4..7] may be parity
0 - high to power card 2 - card data in
1 - high to reset card wake0 - card detect in (low if card)
4 - clock for card
5 - data for card





These holes are for supports for the smartcard reader when a bare board is used



Title: Serial I/O	9 of 16
By: Mark Hayter	
$Date: 1997/08/03 01:57:15 $	
RCS $Revision: 1.34 $	
Version: Rev 5	

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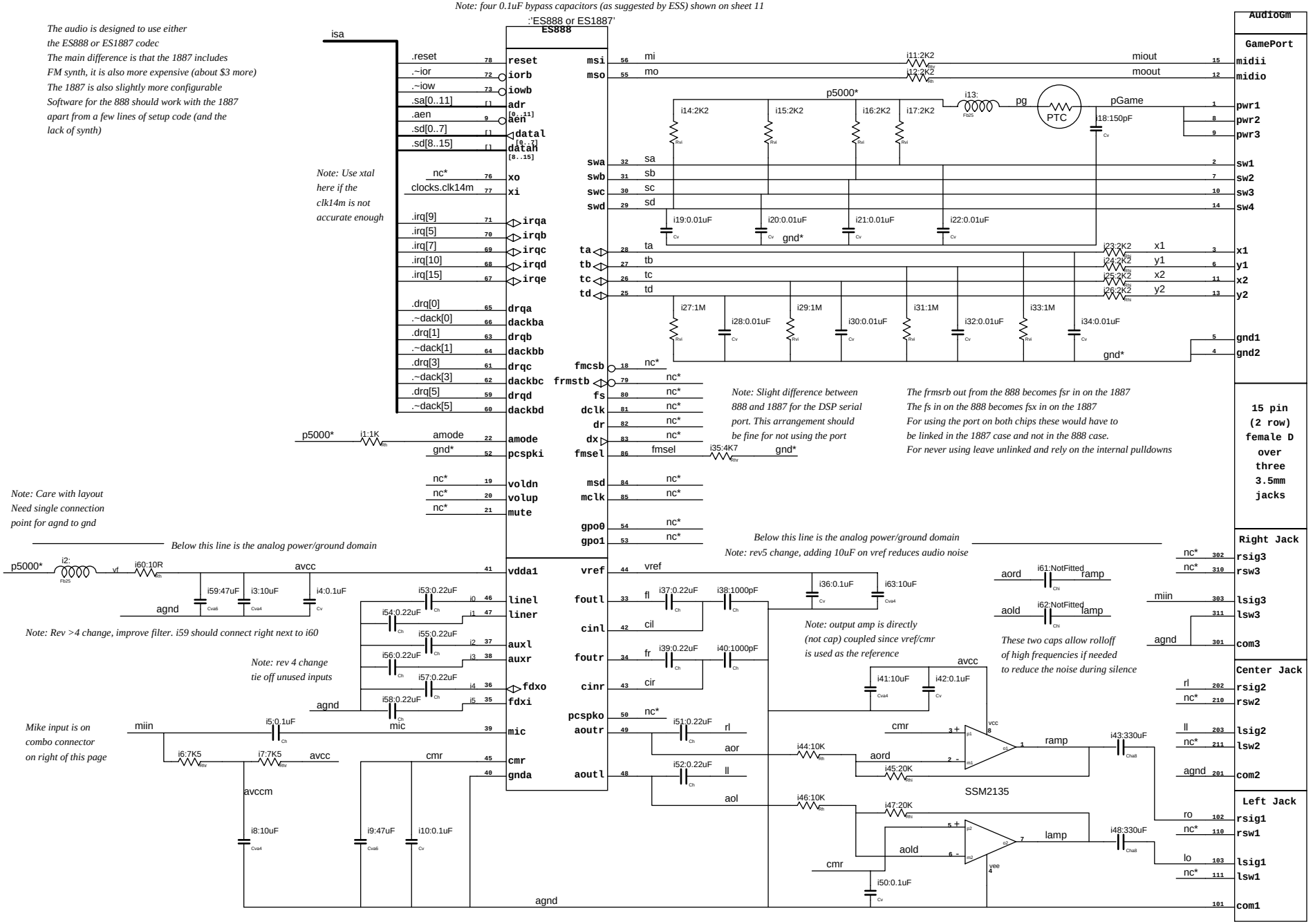
Note: four 0.1uF bypass capacitors (as suggested by ESS) shown on sheet 11

The audio is designed to use either the ES888 or ES1887 codec
The main difference is that the 1887 includes FM synth, it is also more expensive (about $3 more)
The 1887 is also slightly more configurable
Software for the 888 should work with the 1887 apart from a few lines of setup code (and the lack of synth)

:'ES888 or ES1887'



Title: Audio	10 of 16
By: Mark Hayter	
$Date: 1997/08/02 21:50:16 $	
RCS $Revision: 1.35 $	
Version: Rev 5	

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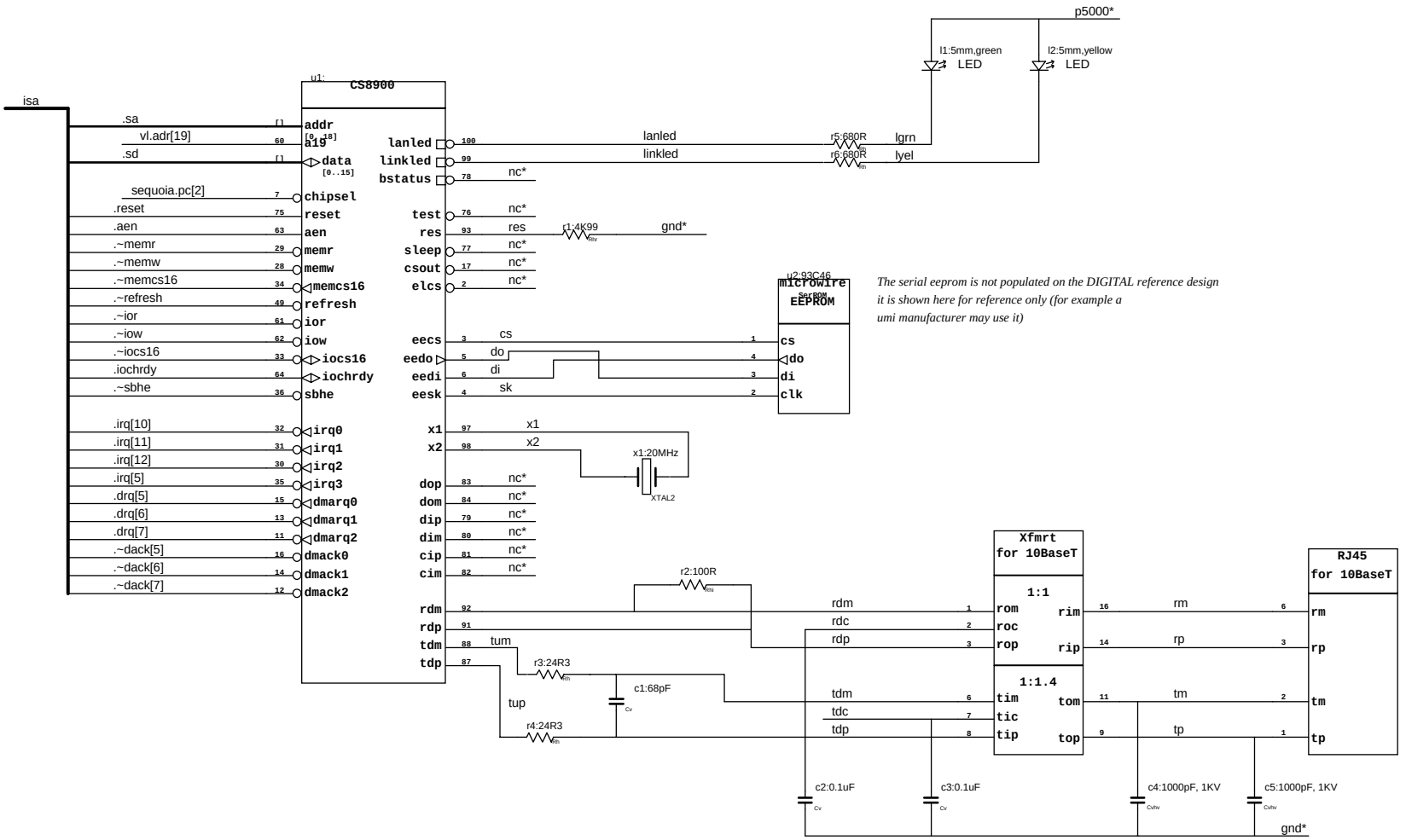

The serial eeprom is not populated on the DIGITAL reference design it is shown here for reference only (for example a umi manufacturer may use it)

Four digital, three analog recomended by Crystal
One for serial eeprom, four for audio (sheet 10)

p5000* — pwr IObypass (sheet14) — 12x0.1uF

R2, R3, and R4 are setup for 100 ohm twisted pair.
Other values are possible. See CS8900 data sheet, page 123.

Note: Changed these caps from 10n to 1n

Title: Ethernet	11 of 16
By: Hal Murray	
$Date: 1997/07/09 18:26:55 $	
RCS $Revision: 1.17 $	
Version: Rev 5	

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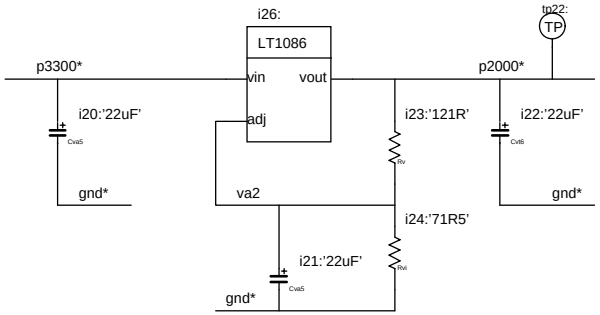
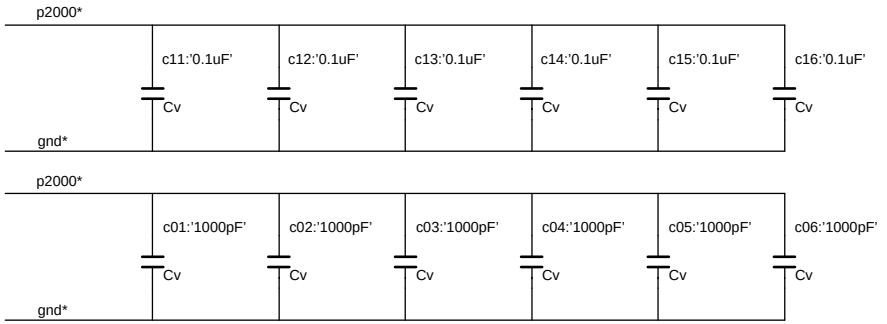
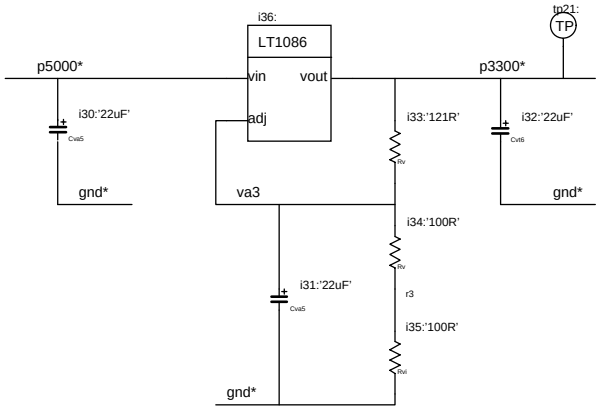
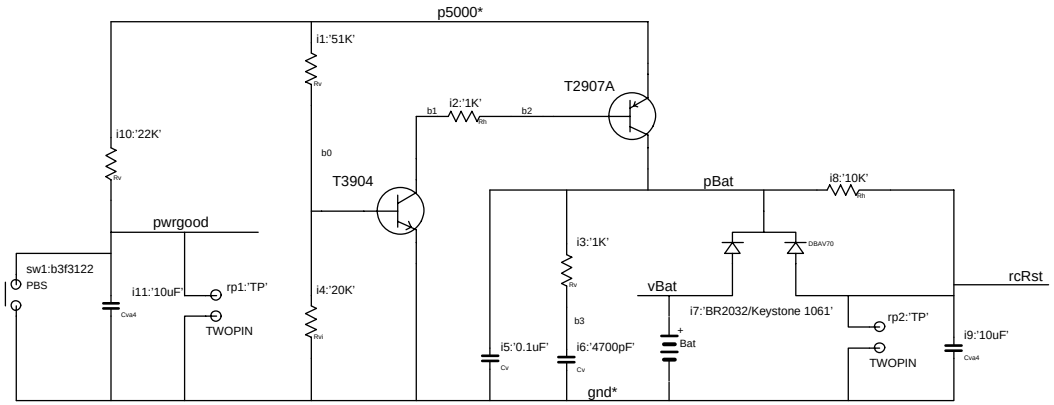
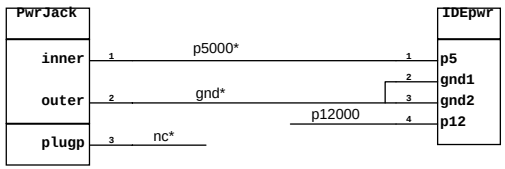


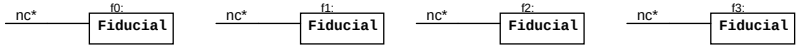




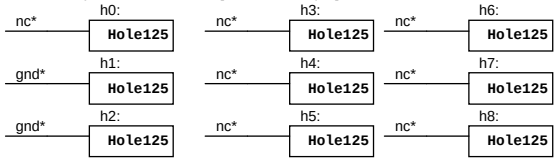


Note: Battery is 3V Li coin cell BR2032 in a smt holder





Note: These are the mounting holes, with the two near the connectors grounded they have a .220 diameter pad with a .125 fhs plated hole



Title: Power	12 of 16
By: Mark Hayter	
$Date: 1997/07/28 04:40:15 $	
RCS $Revision: 1.31 $	
Version: Rev 5	

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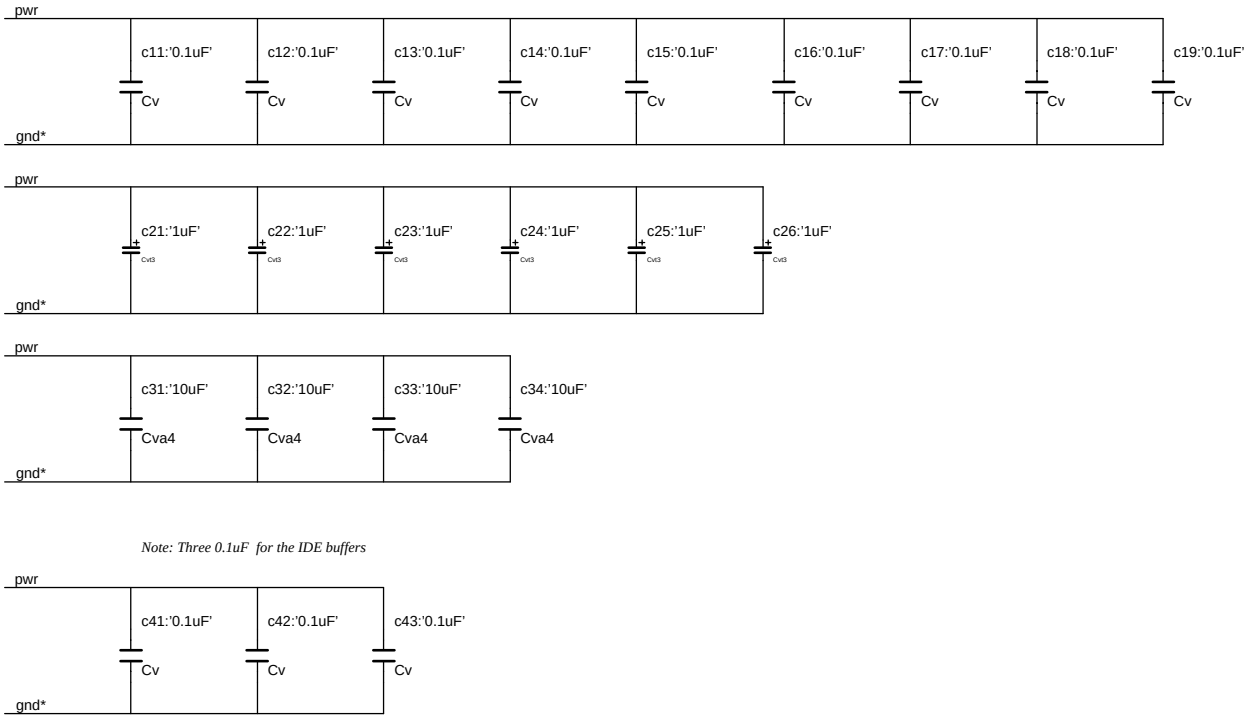
Note: Sequoia1 gets 0.1uF + 1uF for each of the five power groups plus 1uF extra
Note: Sequoia2 gets 0.1uF + 10uF for each of the four power groups



Note: Three 0.1uF for the IDE buffers

Title: Sequoia bypass	13 of 16
By: Mark Hayter	
$Date: 1997/07/09 18:26:55 $	
RCS $Revision: 1.9 $	
Version: Rev 5	

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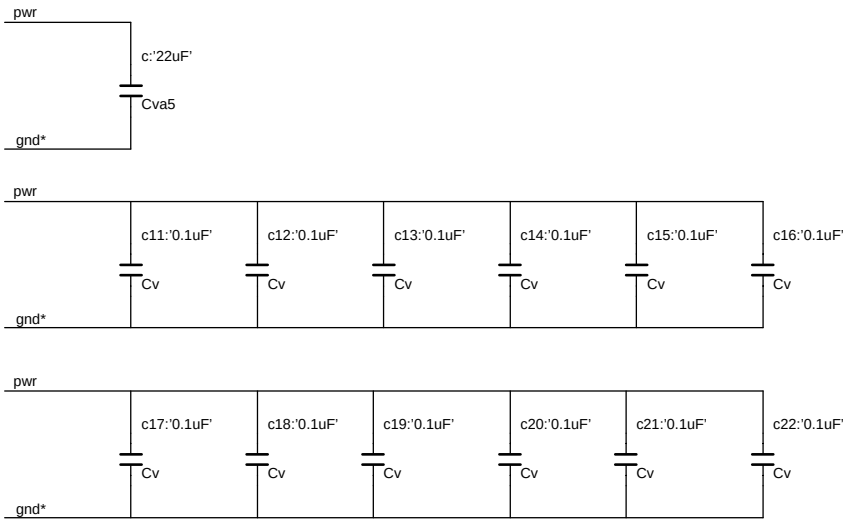

Title: I/O bypass	14 of 16
By: Mark Hayter	
$Date: 1997/07/09 18:26:55 $	
RCS $Revision: 1.9 $	
Version: Rev 5	

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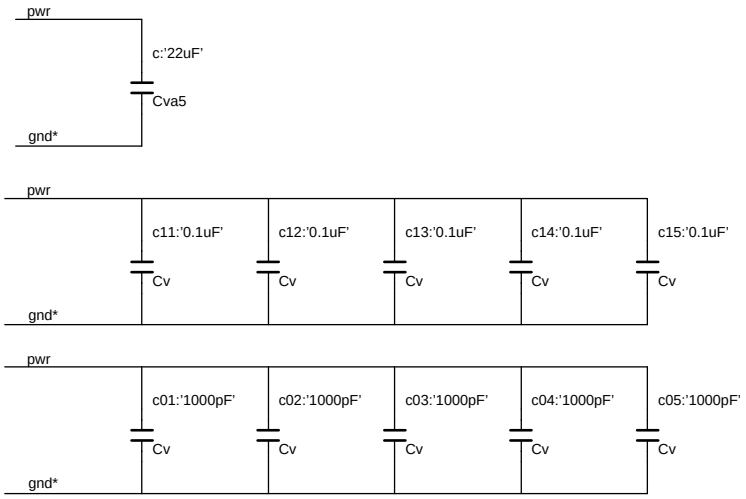

Title: Bypass (5)	15 of 16
By: Hal Murray	
$Date: 1997/07/09 18:26:55 $	
RCS $Revision: 1.9 $	
Version: Rev 5	

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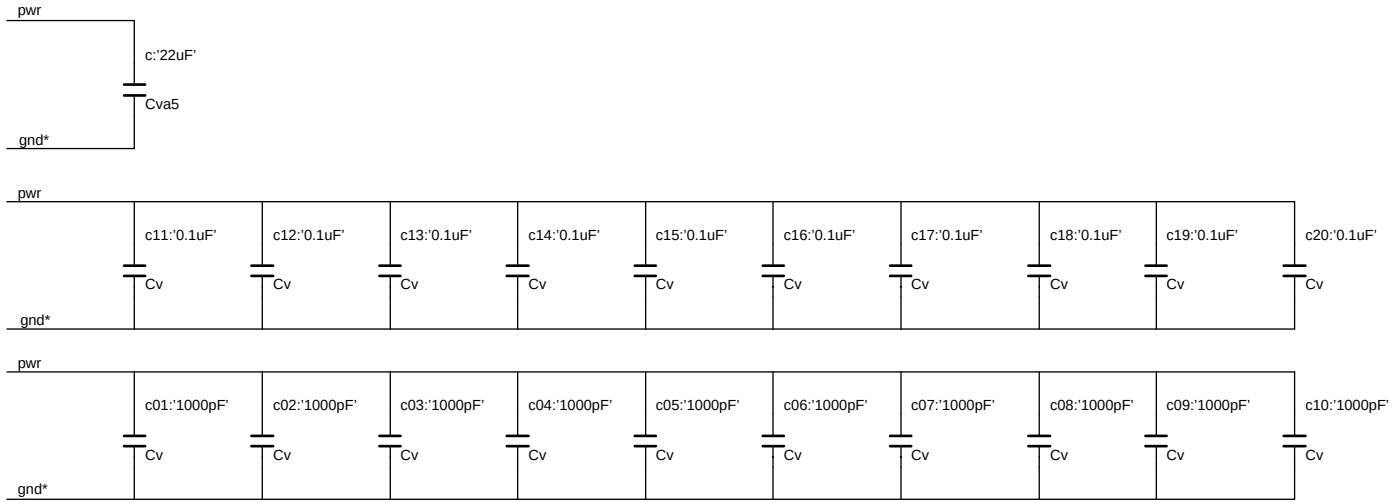

Title: Bypass (10)	16 of 16
By: Hal Murray	
$Date: 1997/07/09 18:26:55 $	
RCS $Revision: 1.11 $	
Version: Rev 5	

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