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ARM Family Expands at EPF

ARM11 Microarchitecture Stretches Pipe to Boost Frequency

By Cary D. Snyder {6/3/02-01}

It has been 11 years since ARM introduced the first ARM6 family of processors based on its first embedded RISC core. Since then, pressure and demand to improve performance have been continuous, so it is fitting that ARM chose to introduce the ARM11 microarchitecture at **Embedded Processor Forum 2002**. The first public presentation of the ARM11 microarchitecture by Ian Devereux, the ARM11 technical lead, revealed how the first microarchitecture implementation using the ARMv6 architecture specification will enable higher-performance ASIC designs using ARM-based cores.

The ARM11 announcement extends the range of ARM's offerings, which had a relatively obscure beginning as a joint venture among Apple Computer, Acorn Computer Group, and VLSI Technology. The ARM6 became the core of Apple's Newton products, and has achieved substantial success in cell-phone designs.

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Ian Devereux introduces the ARM11 microarchitecture at EPF 2002.

ARM11 Implements ARMv6

New details presented on the ARM11 microarchitecture define the internal design and hardware resources necessary to support the ARMv6 architectural specification announced at MPF 2001 (see *MPR 11/26/01-03*, "ARM Drives V6 to MP Forum"). Actual core products, synthesizable cores and hard macros, will be implemented using the ARM11 microarchitecture. A common problem facing ASIC design teams is getting final timing closure with synthesized designs. Timing closure problems are particularly difficult in ASICs having higher-frequency requirements. Compounding the difficulty in meeting strict register-to-register timing are higher clock-frequency requirements and use of synthesis-friendly structures like compiled RAMs. The entire process must support standard ASIC design flows, meaning that a design team cannot use custom logic structures or content-addressable memories (CAMs). ARM's few architectural licensees, such as Intel, can use more elaborate means to achieve design goals.

Devereux's presentation addressed the way the ARM11 microarchitecture will meet customer design-flow and performance requirements. The ARMv6 specification features mixed-endian modes and an enhanced memory subsystem called VMSA v6, which includes two-cycle L1 memory accesses that can support data and instruction caches and tightly coupled memory (TCM). Additional microarchitecture enhancements involve ALU/MAC pipeline extensions, decoupling of the load/store unit (LSU), and addition of dynamic branch prediction (BP) to help minimize prediction penalties.

Outlining a Long Feature List

The ARM11 feature summary starts out with a longer eight-stage pipeline as a single-issue out-of-order-completion CPU

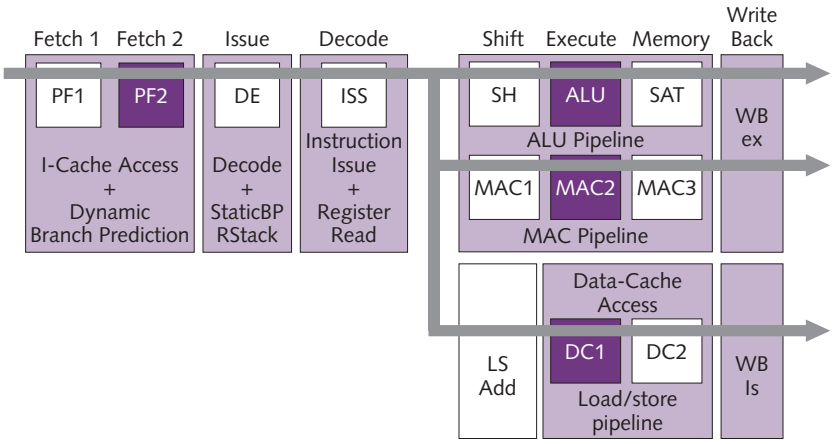

Figure 1. The ARM11 pipeline has eight stages, vs. six in ARM10. Stages highlighted in the darker color were added to permit ARM11 cores to achieve higher clock speeds.

core. Architecturally the ARM11's pipeline has similarities to the six-stage pipeline used in the ARM1026EJ core, but with a pipeline stage added to the instruction fetch and with the execute shift and ALU stage split into two stages (see *MPR 4/30/02-01*, "Exploring the ARM1026EJ-S Pipeline").

The most significant change introduced in the ARM11 microarchitecture is the long eight-stage pipeline. Figure 1 shows the stages that were added to the six-stage ARM10 pipeline. ARM designers used two pipeline stages in the ARM11 microarchitecture to implement two types of branch prediction (BP) and a simple three-entry return stack. The first BP uses a historical record to implement a dynamic branch predictor. A 64-entry, four-state branch-target address cache (BTAC) holds the most recent branch-taken addresses. This dynamic BP adds a classic four-state prediction scheme implementing strongly taken, weakly taken, weakly not-taken, and strongly not-taken states. Dynamically predicted branches are folded into the pipeline, enabling a zero-cycle unconditional branch. A second, static branch predictor handles those branches not found in the BTAC by the dynamic branch predictor. Backward branches are assumed to be loops and are predicted taken; forward branches are predicted not taken. According to ARM, the combined use of pipeline forwarding and prediction techniques improves the pipeline's throughput capability while reducing effective latency to equal that of a five-stage pipeline.

ARM claims its dynamic and static branch prediction accuracy in the ARM11 microarchitecture is approximately 85%; most prediction schemes achieve 80–95% prediction accuracy, depending on program size. The 64-entry BTAC and three-entry return stack represent a reasonable trade-off, given size, power, and performance requirements.

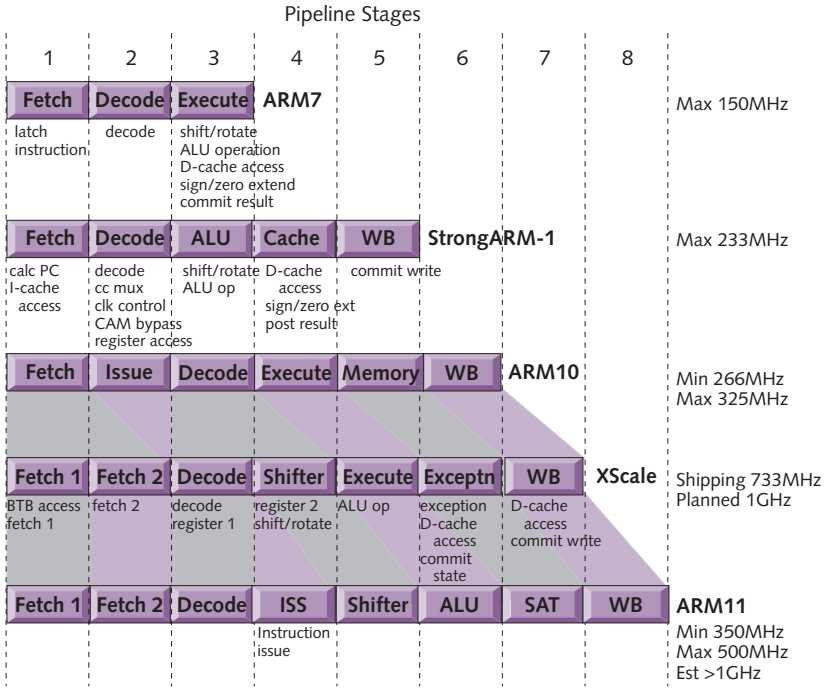

Figure 2. Comparison of ARM architectural pipeline depth starts with ARM7 with three stages, ARM9 and StrongARM with five stages, and XScale with seven stages. It ends with ARM11, which now has an eight-stage pipeline. Maximum claimed and estimated clock frequencies for soft and hard cores are shown on the right.

Two extra stages in the ARM11 pipeline added an extra cycle for instruction-cache (PF1/PF2) and data-cache accesses (DC1/DC2), as shown in Figure 1 and Figure 2. The extra cycles provide extra timing margins that enable higher operating frequencies while easing timing closure as part of an ASIC design flow.

The extra stage also spreads the ALU and MAC pipeline structure over three pipeline stages in the ARM11 microarchitecture, as opposed to two stages in the ARM10. This is particularly important in the synthesis-ASIC design flow, as certain logic structures, like pass and domino logic, are not available: the logic used in building ASICs is typically built from single-edge clocked register-to-register structures.

A new "wait for interrupt instruction" enhances the core's power-management capability. Interrupt latency has been improved over that of previous ARM microarchitectures; latency is now 20 to 30 cycles under worst-case conditions.

The ARM11 will implement the new virtual memory system (VMSA) that is part

of the ARM V6 architecture specification. The new memory system supports nonblocking and hit-under-miss operation. Pipeline execution continues after a cache miss, as long as subsequent instruction execution is not dependent on the missing data: the MMU and caches allow hit-under-miss operation with up to two outstanding misses. The pipeline stalls only after three successive data-cache misses.

The load/store pipeline is decoupled to allow use of a 64-bit datapath for accessing general-purpose registers, providing a method to read or write two register locations per clock cycle. Decoupling the load/store pipeline also permits subsequent instructions to be issued while loads and stores complete in the background. For example, a return from a procedure call completes immediately and starts the next execution cycle while the associated store operation is completed at the same time.

Boosting Synthesizable Core Frequencies

The ARM11 microarchitecture was designed to achieve higher operating frequencies than previous ARM cores. According to ARM, the increase to eight pipeline stages will allow ARM11-based cores to operate at 350MHz to 500MHz, worst-case, in 0.13-micron silicon technology. For example, an ARM11-based soft core, implemented using TSMC's C013G process technology—a generic 0.13-micron process—is expected to hit a 350MHz (slow silicon, V_{dd}-10%, 125∞C) operating frequency. The same core, implemented in TSMC's C013LV low-voltage 0.13-micron process technology, is expected to achieve 420MHz under the same conditions. The highest expected operating frequency of 500MHz will require an ARM11-based hard core on the same TSMC C013LV process technology; initial 500MHz ARM11-based implementations will come from ARM's hard-macro core-development program. ARM expects that its customers, using the right manufacturing strategy, will be able to screen parts and get production-quantity yields of parts that can operate at more than 700MHz. ARM believes the ARM11 hard core could exceed 1GHz using 90nm process technology.

Price & Availability

The first validation part built using the ARM11 microarchitecture will be taped out in Q402.

Evolution of the ARM Microarchitecture

ARM has maintained tight control over the ARM architecture and has only two architectural licensees, whereas MIPS Technologies has twelve. ARM needs its own set of products that can hit 1GHz clock frequencies and higher (Intel is close to shipping its 1GHz XScale parts), and, to do this, it had to take the big step and extend its pipeline depth. ARM finally has a microarchitecture that has more pipeline stages than XScale's seven-stage pipeline. Figure 2 relates the ARM architectures' pipeline depth to maximum obtainable operating frequencies.

The ARM11 microarchitecture defines the hardware that will implement the 83 new instructions defined in the ARMv6 architectural specification. A large number of the new instructions are new 8- and 16-bit SIMD operations. Many features implemented in the ARM10 cores have been refined and incorporated into the ARM11 microarchitecture: for example, the improvements in the ARM1026EJ's static branch prediction logic and return stack have found their way into the ARM11 feature set.

Software compatibility and ARM instruction-set architecture (ISA) stability are important to long-time users, and ARM is making its new ARM11 architecture 100% upward compatible with previous architectures. The binary-compatible architectures include the ARMv4 architecture used by ARM7 and StrongARM cores and the ARMv5TE architecture implemented in the ARM9E, ARM10, and XScale cores. The new ARMv6 architecture starts with the ARM11 family of

		StrongARM	ARM9E	ARM10E	XScale	ARM11
Architecture		ARMv4+	ARMv5TE(J)	ARMv5TE(J)	ARMv5TE+	ARMv6
Pipeline Length/Stages		5	5	6	7	8
No. of Thumb Instr		n/a	Base	Base	Base	Base+6
Media Instructions		No	No	No	Yes	Optional Coprocessor
Java Decode		No	ARM926EJ	ARM1026EJ	No	Yes
V6 SIMD Instr		No	No	No	No	Yes
Memory Mgmt		Custom	MSA v5	MSA v5	Custom	VMSA v6
Branch Pred		No	No	Static	Dynamic	Dynamic
Independent Load/Store Unit		No	No	Yes	Yes	Yes
Concurrency		None	None	ALU/MAC, LSU	ALU/MAC, LSU	ALU/MAC, LSU
Out-of-order completion		No	No	Yes	Yes	Yes
Target Implementation		Custom Processors	Synthesizable Core	Synthesizable Core	Custom Processors	Synthesizable & Hard macros
Target Freq	Fixed/Custom	233MHz	n/a	325MHz	1GHz	500MHz – >1GHz
	Synthesizable	None	250MHz	325MHz	None	420MHz

Table 1. ARM architecture feature comparisons for ARM Ltd.- and Intel-licensed architectures. The "+" designates custom media instructions that were added to the base architecture. n/a = not available

products. Table 1 lists the key characteristics of the ARM9, ARM10, and ARM11 architectures.

ARM Marches On

The first soft-macro ARM11-based core should be available by the end of the year. The operating frequencies these products will achieve using standard ASIC design flows and commercially available silicon process technologies are unknown, but ARM expects these implementations to achieve frequencies up to 420MHz.

Over the past 10 years, ARM has demonstrated its ability to evolve its architecture. We believe the ARM11 microarchitecture has the features and performance the market needs, and expect it to achieve greater success.

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